Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (Currently amended) An integrated circuit comprising:

a control block comprising:

a first series of delay elements coupled to a reference clock input;

a phase detector coupled to the reference clock input and an output of the first series of delay elements; and

a counter having an input coupled to an output of the phase detector and an output coupled to control inputs of the first series of delay elements;

a storage circuit having an input coupled to the output of the counter; and

a delay circuit having a control input coupled to an output of the storage circuit,

wherein the delay circuit comprises a series of delay elements, each having an input and an output, and

wherein the storage circuit comprises a logic gate coupled to an input of a delay element in the delay circuit and an output of a delay element in the delay circuit, and further coupled to a latch, the latch coupled between the counter in the control circuit and the delay circuit.

Claim 2. (Original) The integrated circuit of claim 1 wherein the storage circuit comprises a plurality of flip-flops having an input coupled to the counter in the control block, an output coupled to the delay circuit, and a clock input coupled to an output of the delay circuit.

Claim 3. (Original) The integrated circuit of claim 1 wherein the storage circuit comprises:

a logic gate coupled to an input and the output of the delay circuit, and further coupled to a latch, the latch coupled between the counter in the control circuit and the delay circuit.

Claim 4. (Cancelled)

Claim 5. (Currently amended) The integrated circuit of claim [[4]] 1 wherein the logic gate is an exclusive-OR gate.

Claim 6. (Original) The integrated circuit of claim 1 wherein the delay circuit is a delay element.

Claim 7. (Previously presented) The integrated circuit of claim 6 further comprising:

a first register having a clock input coupled to the output of the delay circuit; and

a second register having a complementary clock input coupled to the output of the delay circuit.

Claim 8. (Original) The integrated circuit of claim 7 wherein the first register has a first input and the second register has a second input, and the first and second inputs are coupled to a data input.

Claim 9. (Original) The integrated circuit of claim 8 wherein the integrated circuit is a field programmable gate array.

Claim 10. (Currently amended) An integrated circuit comprising:

a control circuit to receive a reference clock and provide a plurality of control bits, wherein the control circuit comprises:

a first series of delay elements to receive the reference clock;

a phase detector to compare the phases of the reference clock and an output of the first series of delay elements and provide an output signal; and

a counter to receive the phase detector output signal and provide the control bits;

a storage circuit coupled to receive and store the plurality of control bits, and further to provide the plurality of stored control bits; ~~and~~

a delay element to receive the plurality of stored control bits, and to provide a clock signal to the storage circuit; and

a second series of delay elements including the delay element, each delay element in the second series of delay elements having an input,

wherein the storage circuit comprises a logic gate to receive a signal from an input of a delay element in the second series of delay elements and an output of the second series of delay elements, and further to provide an output to a plurality of latches, each latch to receive and store one of the plurality of control bits, and further to provide the stored one of the plurality of control bits to the delay element.

Claim 11. (Cancelled)

Claim 12. (Currently amended) The integrated circuit of claim ~~11~~ 10 wherein a polarity of the phase detector output depends on the relative phase of the reference clock and the output of the first series of delay elements, and the counter is an up-down counter that counts up when the phase detector output has a first polarity, and counts down when the phase detector output has a second polarity.

Claim 13. (Previously presented) The integrated circuit of claim 10 wherein the storage circuit comprises a plurality of flip-flops, each flip-flop having an input to receive and store one of the plurality of control bits, and further to provide the stored one of the plurality of control bits to the delay element.

Claim 14. (Previously presented) The integrated circuit of claim 13 wherein each of the plurality of flip-flops in the storage circuit has a clock input to receive the output of the delay element.

Claim 15. (Cancelled)

Claim 16. (Currently amended) The integrated circuit of claim ~~15~~ 10 wherein the logic gate comprises an exclusive-OR gate.

Claim 17. (Original) The integrated circuit of claim 10 wherein the control circuit is a delay-locked loop.

Claim 18. (Currently amended) A method of delaying a data strobe signal comprising:

receiving a reference clock signal;

delaying the reference clock signal a first duration, the first duration dependent on a plurality of control signals;

comparing the phase of the reference clock signal and the delayed reference clock signal to generate the plurality of control signals;

storing the plurality of control signals;

receiving a data strobe signal; and

delaying the data strobe signal a second duration, the second duration dependent on the plurality of stored control signals,

wherein the control signals are not stored while the data strobe signal is delayed, and wherein the plurality of control signals are stored when an edge of the data strobe signal is not being delayed.

Claim 19. (Original) The method of claim 18 wherein the plurality of control signals are stored when the received data strobe signal has been delayed the second duration.

Claim 20. (Cancelled)